MNT genierie 2017

Technology for Radio-Frequency Phononics

or, rather,
An Unofficial Introduction to Microfabrication

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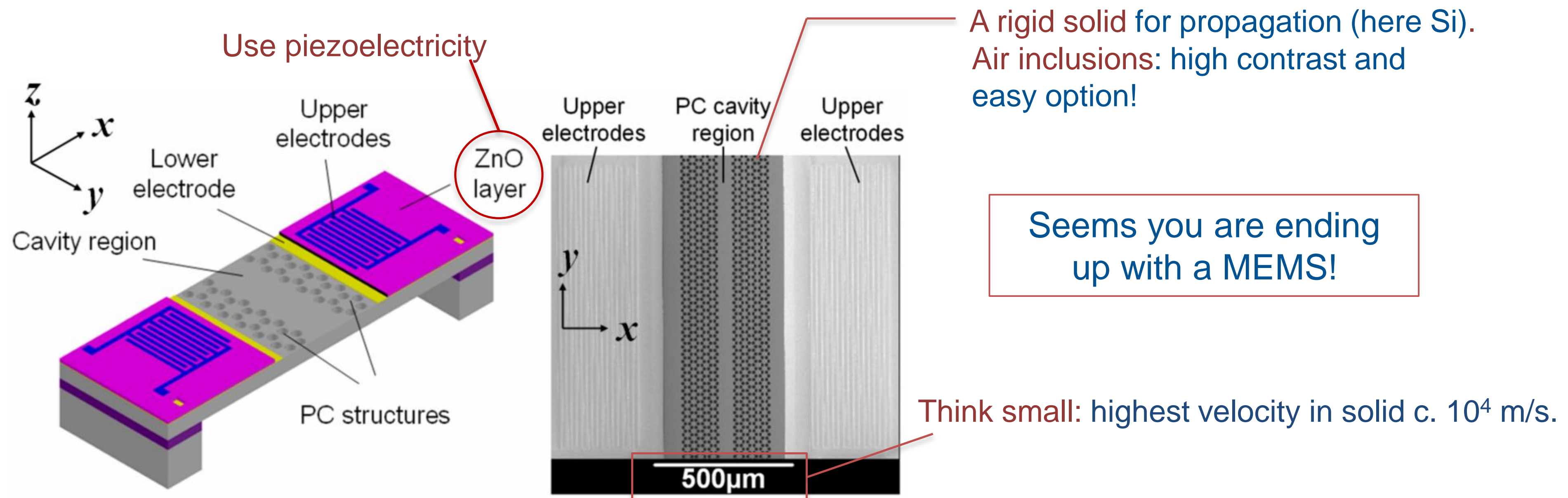
Acknowledgments

- Franck Chollet, FEMTO-ST, Université de Bourgogne Franche-Comté.
- Sam Zhang and Liu KuoKang, Nanyang Technological University.
- Marc Solal's Lecture Notes at ENSMM, Besançon.
- A Hands-on Introduction to Nanoscience: www.virlab.virginia.edu/Nanoscience_class/Nanoscience_class.htm
- R. Bruce Darling's Lecture Notes, University of Washington.
- Marc J. Madou, *Fundamentals of Microfabrication*, CRC Press (2002).

How to build a RF phononic crystals?

The same way you would build an audible, or a ultrasonic one or a sismic one… except that you make it smaller!

- A medium of some sort to support elastic wave propagation ;
- A way to get at least two materials with contrasting elastic properties arranged periodically ;
- Embedded elastic wave source and detectors if you really want to go « device » ;
- All this in the 100 MHz – few GHz frequency range.



S. Mohammadi; A. A. Eftekhar; W. D. Hunt; A. Adibi, *Appl. Phys. Lett.* **94**, 051906 (2009).

Aim of the course

Introduce some notions of microfabrication that may be used for phononic crystal fabrication

- Basic notions on clean room processing.
- I will heavily insist on patterning.
- Some examples of subtractive and additive processes.
- Scales and dimensions.

Try to present them in the context of:

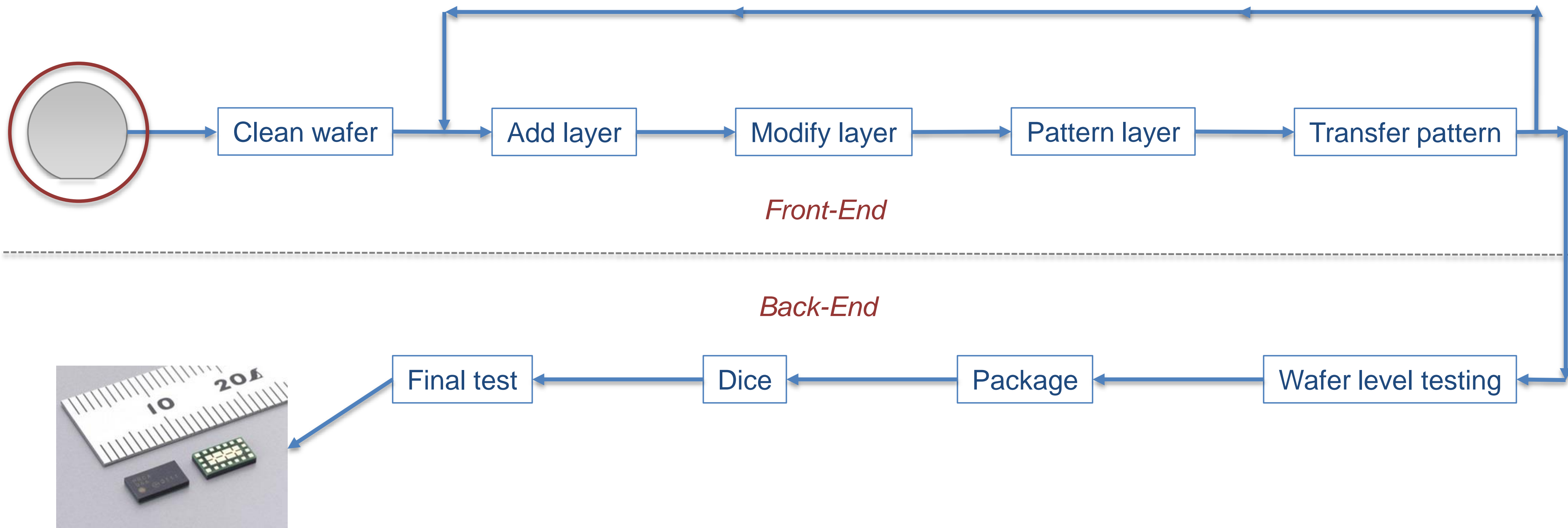
- Conventional SAW and BAW device fabrication.
- RF phononic crystals.

These lecture notes are obviously absolutely not exhaustive and cannot be always considered as accurate (a few liberties and shortcuts taken…)

A very short intro to MEMS

A typical MEMS technological process

- Finds its roots in planar processes used for integrated circuits fabrication: simple batch fabrication of devices with ever tinier feature size.
- Can be described as a series of basic steps combined and repeated many times on a substrate.

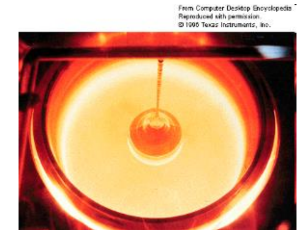


Murata Manufacturing Co., Ltd

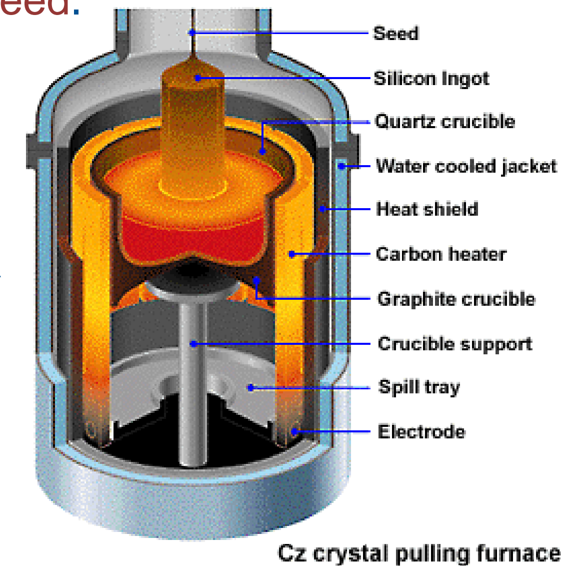
Wafer

For ICs, silicon, obviously

- Single crystal Si grown from an ultrapure polycrystalline Si source through the Czochralski method.
  - Melting at high temperature (1500˚C) under inert gases;
  - Seeding: a small chemically etched seed crystal of about 0.5 cm in diameter and 10 cm in length is lowered into contact with the melt;
  - Pulling: the surface tension between the seed and the molten silicon causes a small amount of the liquid to rise with the seed and cool into a single crystalline ingot/boule with the same crystallographic orientation as the seed.



- The silicon ingot diameter is determined by a combination of temperature and extraction speed.
- Most ingots produced today are 150mm (6") and 200mm (8") diameter.



Cz crystal pulling furnace

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Wafer fabrication

- The ingot is sliced into individual wafers with a precision "Inner Diameter Saw".
- The wafers are mechanically lapped and etched in a wet chemical solution to remove microscopic cracks or surface damage, then thoroughly cleaned in high-purity DI water baths.
- The wafers eventually are polished through Chemical Mechanical Polishing (CMP).
- Wafer characteristics:
  - Diameter
  - Thickness
  - Orientation, i.e. the growth plane of the fabricated single crystal described using Miller indices such as (100), (111), (110) and indicated with a "flat" – we will get back to this later…
  - Polish: single-side, double-side, quality of surface finish.
  - Bow/warp: deviation from the plane of the wafer centerline.
  - TTV – total thickness variation.
  - + conductivity, resistivity (depends on doping)

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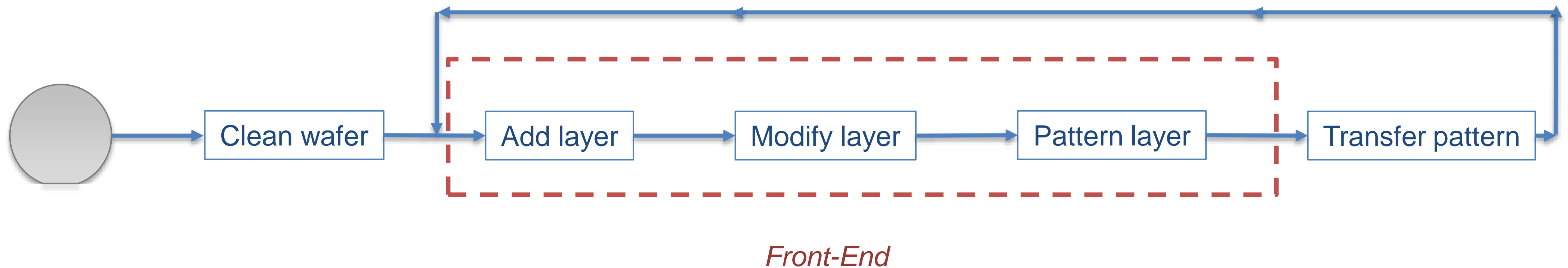
Patterning



The key concept behind microfabrication

- Idea: shape the material of interest into the desired pattern at the micron scale.
- Very few techniques allows for a direct drilling/milling of the materials (Focused ion beam milling is one noticeable exceptions, found in the Phononics literature)
- Need for a work around:
  - Use a protective surrogate layer that can be easily patterned and subsequently removed.
  - Transfer the pattern to the material of interest.

Photolithography

A wee bit of History

- 1820s: Heliography. Nicéphore Niépce (Chalon-sur-Saône, France), used Bitumen of Judea, an acid resistant, photosensitive natural asphalt to produce the first permanent photographic image. Dissolved it in lavender oil for coating and exposed it to sunlight through an engraving.
- 1826: Nicéphore Niépce used a camera obscura for exposure.

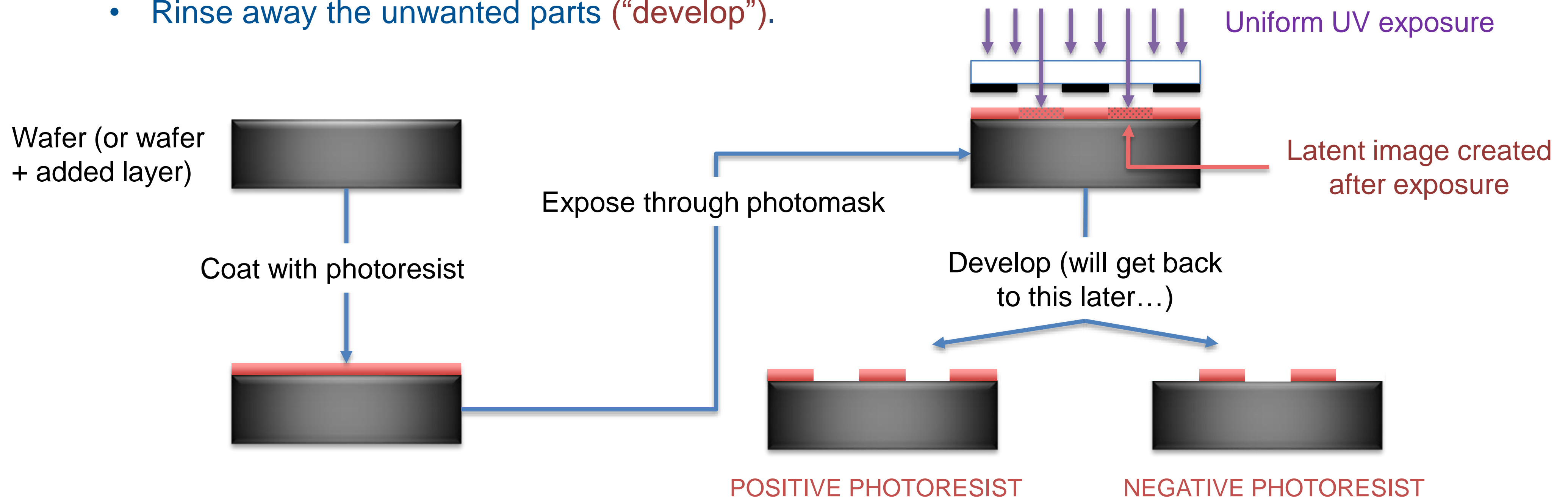
- 1935: Louis Minsk (Eastman Kodak Company) develops the first negative photoresist.
- 1940: Otto Süss (Kalle Div. of Hoechst AG) develops the first positive photoresist using diazonaphthoquinone.

Same process as the one used for printed circuit board fabrication, except with higher resolution (and except that the PCB are already pre-coated with photoresist!)

Photolithography

… or optical lithography or UV lithography

- Use light (UV illumination) to transfer a geometric pattern onto the surrogate layer:
  - Surrogate layer needs to be light-sensitive and needs to exhibit good chemical resistance: “photoresist”;
  - Expose through a mask (a “photomask” or “reticle”) that displays the desired pattern through clear and opaque areas;
  - Rinse away the unwanted parts (“develop”).



Photolithography

Photolithography is the most common measure of the complexity of a technological process.

- Number of masks reflects the number of technological steps and of added/subtracted layers (lithography represents about 50% of the process steps).
- The mask fabrication/exposure process sets the minimum feature size.
- Lithography is the most demanding process and drives the entire infrastructure. Reaching small feature sizes requires:
  - Cleanliness;
  - Controlled room temperature and humidity;
  - A vibration-free environment.
- Metrics (industrial standards)
  - Resolution.
  - Throughput.
  - Alignment (registration).

Overview of the photolithography process

Surface preparation
↓
Coating
↓
Soft-bake
↓
Mask Alignment
↓
Exposure
↓
Post-exposure bake
↓
Flood exposure
↓
Development
↓
Hardbake

Clean to remove:

- Dust of any sort;
- Abrasive particles from CMP;
- Lint from wipers;
- Bacteria;
- Any residues from previous process steps (resist, solvent, even water…)

What is a photoresist (PR)?

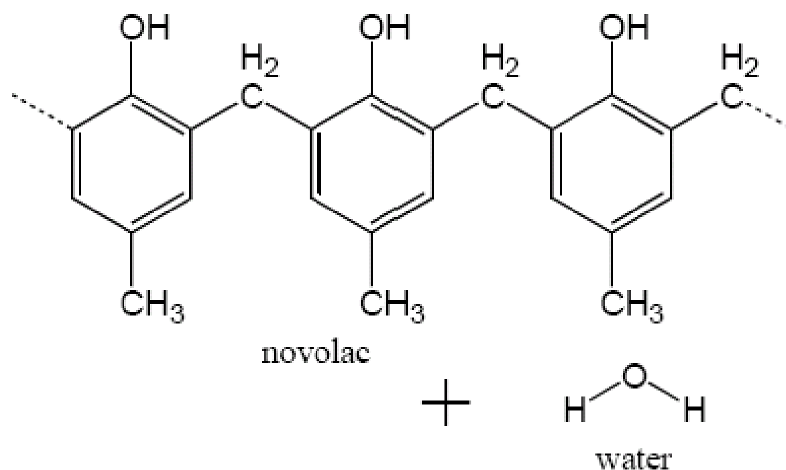
A mixture usually composed of:

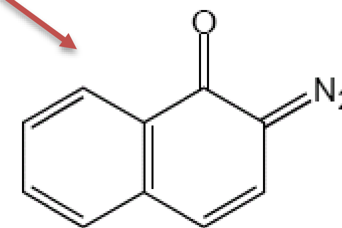
A resin or base material
ensures good chemical and mechanical resistance of the photoresist.

A photoactive compound (PAC)
An additive sensitive to UV radiation that helps to create chemical change in the resin. Some resin don't need this compound as they are directly sensitive to UV radiation.

A solvent
Keeps the solution liquid and controls its mechanical properties such as viscosity so that it can be coated easily.

Phenol formaldehyde resin (novolac, monomer)



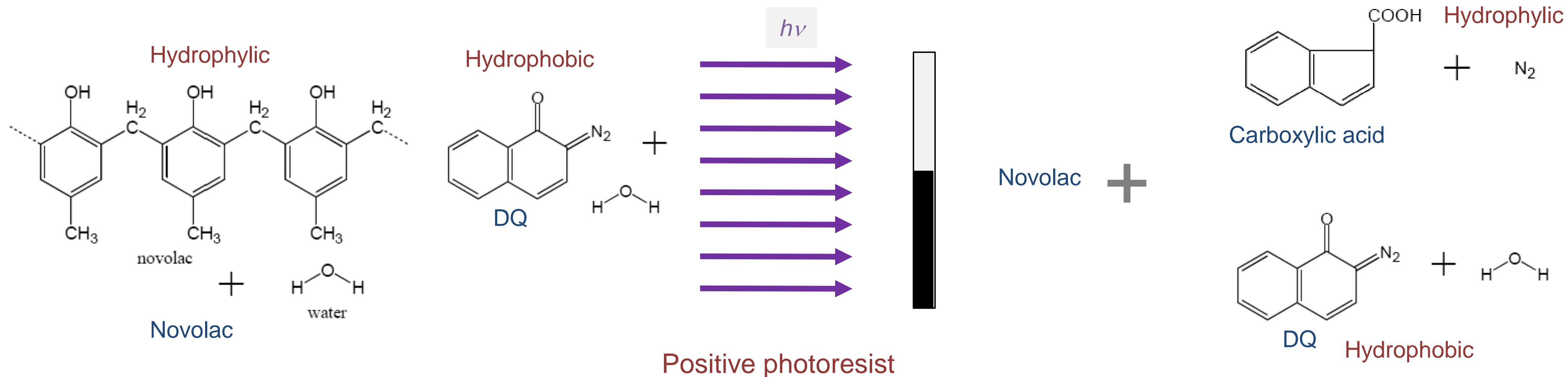


Diazonaphthoquinone (DQ)
(yes, the same as in the 40's!)

Negative vs positive tones

Patterning

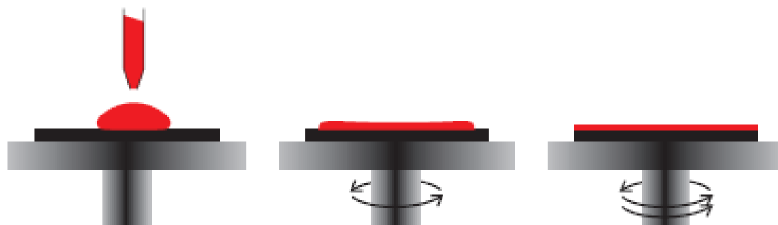
- In negative photoresist the exposure to UV induces cross-linking of the polymer making it less soluble in the developer.
- In positive photoresist the UV exposure creates conditions that increase the dissolution rate of the resin.
- Novolac is the most common type of photoresist currently used. Its dissolution rate is greatly increased in the presence of carboxylic acid.
- Chemically amplified photoresists are based on a two stages reaction that modifies the resin even with little UV exposure. They are generally of the negative type (e.g. SU8).



Positive photoresist

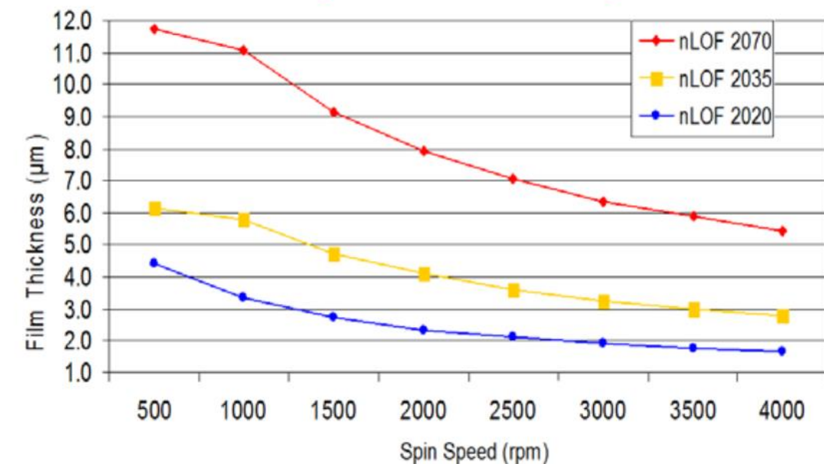
Resist coating

- The coating of the photoresist is performed with a spin-coater, a high speed rotary platform that uses centrifugal forces to obtain a uniform layer on the surface of the wafer.
- The complete process has usually three main steps:
    - Photoresist dispensing in the center;
    - Photoresist spreading at medium speed;
    - Photoresist coating at high speed to achieve the desired thickness.



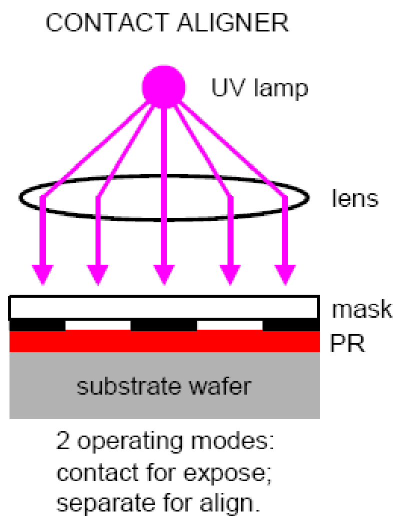
Both manual and automated options, obviously…

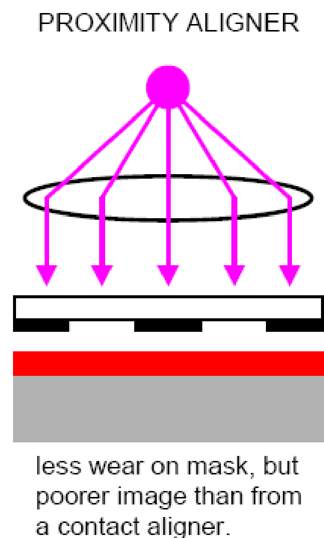
- The final thickness depends on the photoresist viscosity, the spinning rate and to a lesser extent to the nature of the substrate ('sticky' substrate will have thicker layer).
- In general the speed/thickness relationship is given by a series of graph by the photoresist manufacturer.

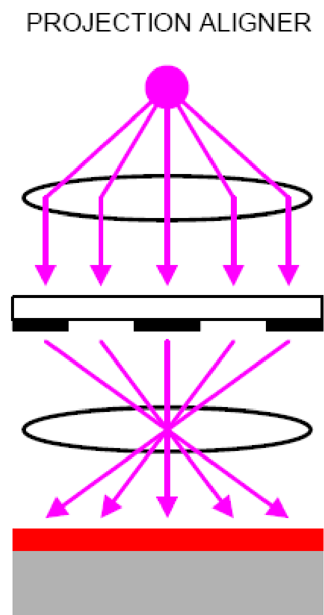


Exposure

- A soft-bake, usually performed above 100°C is used to remove most of the solvent in the initial photoresist mixture.
- Then follows the exposure through the photomask:
  - The wafer is aligned with the mask using a mask aligner (for manual, academic versions) or a stepper (a huge, expensive industrial version).
  - The dose of exposure (impinging energy) determines the dissolution rate of the resist in the developer.
  - There are three main ways to perform exposure:







Very, very cleverly designed and well controlled optics. Stacks of lenses in a tightly controlled environment.

Exposure

- Contact lithography: the resist-coated wafer is in physical contact with the mask. High resolution is possible (< 1 µm, even lower with DUV sources) but debris, trapped between the resist and the mask, may damage the mask.

- Proximity lithography: a small gap, 10 to 25 µm wide, is kept between the wafer and the mask during exposure. This gap minimizes mask damage but decreases resolution.

- Projection lithography: image of the mask is projected onto the resist-coated wafer, which is many centimeters away.

    - Projection systems give the ability to change the reproduction ratio. Going to 5:1 or 10:1 reduction allows larger size patterns on the mask, which is more robust to mask defects and allows increasing the resolution.

    - This method can be used as most wafers contain an array of the same pattern, so only one cell of the array is needed on the mask. This system is called Direct Step on Wafer (DSW). These machines are also called “Steppers”.

Resolution

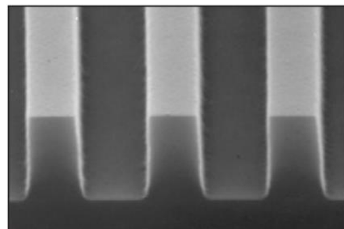
- Photolithography uses optics: diffraction limits the resolution of the exposure system as it 'enlarges' the apertures.
- To increase the resolution, classical optics rules:
  - Decrease the wavelength.
  - Increase the numerical aperture of the objective (this however badly affects the depth of focus of the system and complicates the micro-fabrication).
- Contact UV lithography: Hg lines (g-line: 436 nm, h-line: 405 nm, i-line: 365 nm → 0.8 – 1 μm.
- Contact DUV lithography: ~ 200 nm (248 nm) → 0.5 μm.
- Stepper projection lithography: excimer sources, 248 nm, 193 nm → 100 nm.
- And if you want lower feature sizes:
  - Electron-beam lithography:
    - Resolution ~ 10-20 nm but low throughput, used for photomask fabrication but cannot be used for mass production or in big, big foundries.
  - Excimer sources + immersion lenses + multiple patterning + optical phase masks + clever photochemistry.
    - The standard in the microelectronics industry. Currently <50 nm!

Choice of photoresist

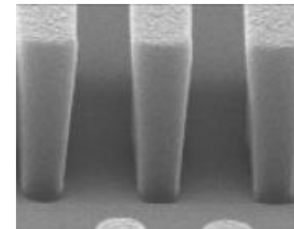
The choice of PR depends on :

- The wanted resolution: aspect ratio limits the useable photoresist thickness. We will see that this is a very important matter for pattern transfer.
- Its adhesion/durability/removal properties
  - Usually, photoresists are used as surrogate layers and are aimed at being removed. There are however noticeable exceptions, e.g. SU8 that is well known and used in microfluidics applications or for its interesting mechanical properties.
- The wanted sidewall profile
  - Obtained by a careful tuning of exposure dose and development.
  - Chosen in relation with the process step to follow, but we will come to that later…

''Normal'' positive resist, slight overcut.



MICROPOSIT™ S1800™ SERIES



AZ® nLOF™ 2000 Series

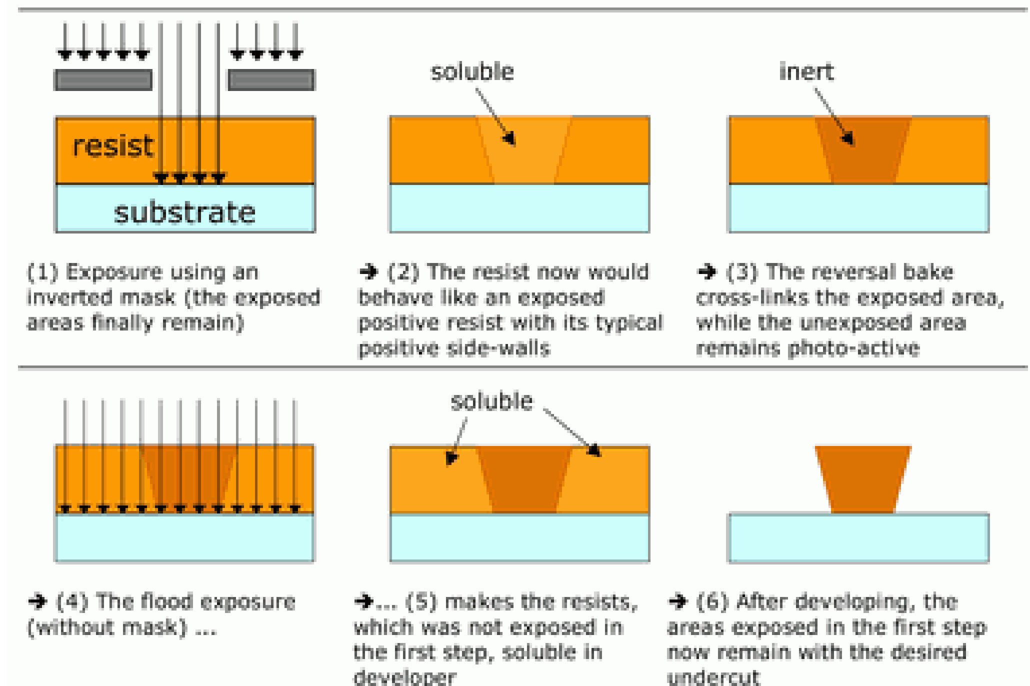
I/R, negative ''lift-off'' resist, Undercut.

- Positive PR are often preferred over negative PR as they are simpler to process/remove.

Image Reversal Photoresists

- Invertible photoresists change polarity after an additional inverting bake. There main interest is that they give negative (re-entrant) profile with positive photoresist.

- Typical process :
  - Soft-bake, as for any resist.
  - 1st UV exposure with mask: exposed photoresist becomes more soluble in developer.
  - Reverse bake: hardens the exposed resist and makes it less soluble in developer.
  - 2nd UV exposure (flood without mask): makes the originally masked photoresist soluble in developer.
  - Development: removes the originally masked photoresist.



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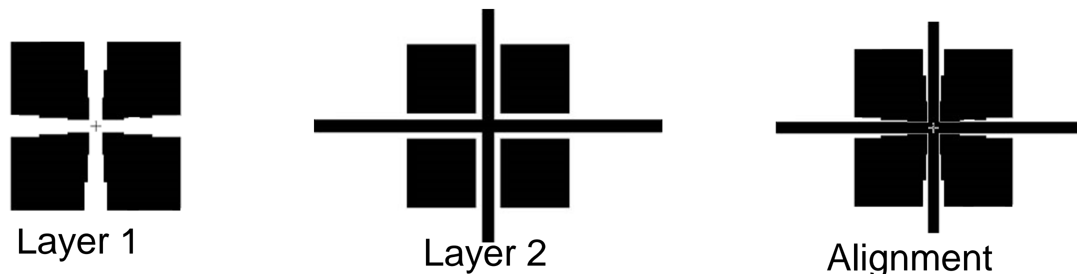
Development & Stripping

- Development
  - Nearly all positive resists use alkaline developers such as KOH or TMAH (tetramethylammonium dioxide) dissolved in water.
  - Negative resists usually develop with organic solvent (PGMEA…).
  - Care must be taken to constantly replenish the developer if a consistent process is to be maintained.
- Removal/Stripping
  - Generally through solvents, although dry processes may be used
    - Acetone is often used although it is in fact not that well-suited as a stripper: the high vapor pressure of acetone causes fast drying and thus re-deposition of stripped photoresist.
    - NMP (1-Methyl-2-pyrrolidon) is a powerful stripper: yields low vapour pressure, strongly dissolves organic impurities as well as resists, keeps the removed resist in solution, and can be heated to 80°C thus improving the performance as remover.

Mask fabrication and layout

It is not only about designing a structure with the largest ever band gap of the fanciest effective elastic properties, it is also about designing a device you can actually build!

- Mask layout is an image of both your design simulation results and your technological process. It integrates everything, from the physics of your problem all through the packaging!
- It has to integrate the technological constraints and the technological step sequence wisely.
- Hence, design, sketch, and use a layout editor to make things real:
  - Layout editor: specific software dedicated to mask design that allows drawing all the patterns superimposed, hence allowing to transpose the successive technological steps. Each of these layer corresponds to a different physical mask.
  - The final step is therefore to include on each layer alignment marks to allow aligning the different layers together



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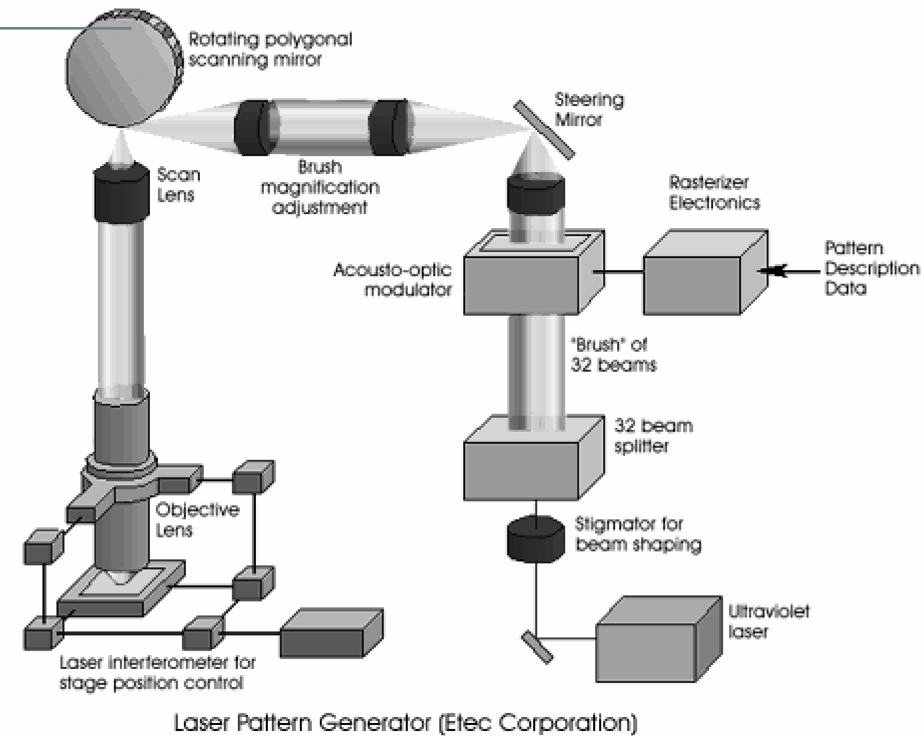
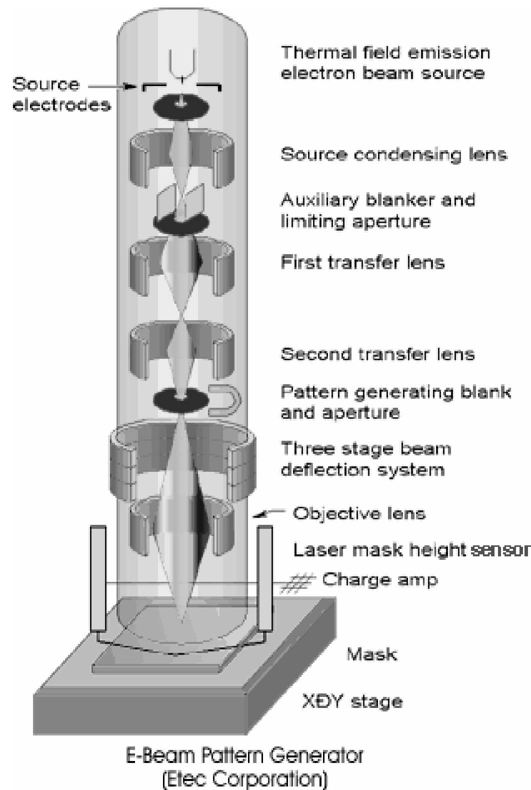
Pattern Generator

- A photomask simply consists of a piece of transparent material (soda lime, quartz) coated with an opaque chromium layer and pre-coated with PR.
- Patten generation occurs through exposure of the PR coated substrate through beam raster scanning. It is a serial process!



Laser Pattern Generator (Etec Corporation)

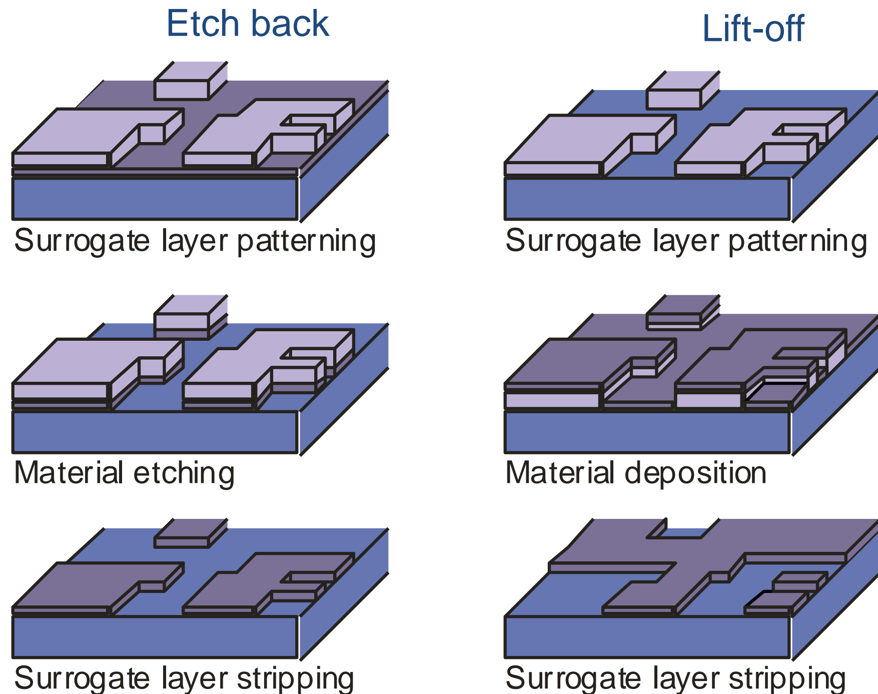


E-Beam Pattern Generator (Etec Corporation)

- Two main beam technologies for the exposure:
  - E-beam: uses scanning focused electron beam, multi-beam systems reaching the market. Generally associated with dry etching.
  - Laser: uses scanned multi-spot focused laser beam, resolution ~1 µm

Pattern Transfer

- In general, the patterns obtained by photo-patterning in the photoresist layer need to be transferred to the desired material.
- There are two main techniques used to perform the pattern transfer:



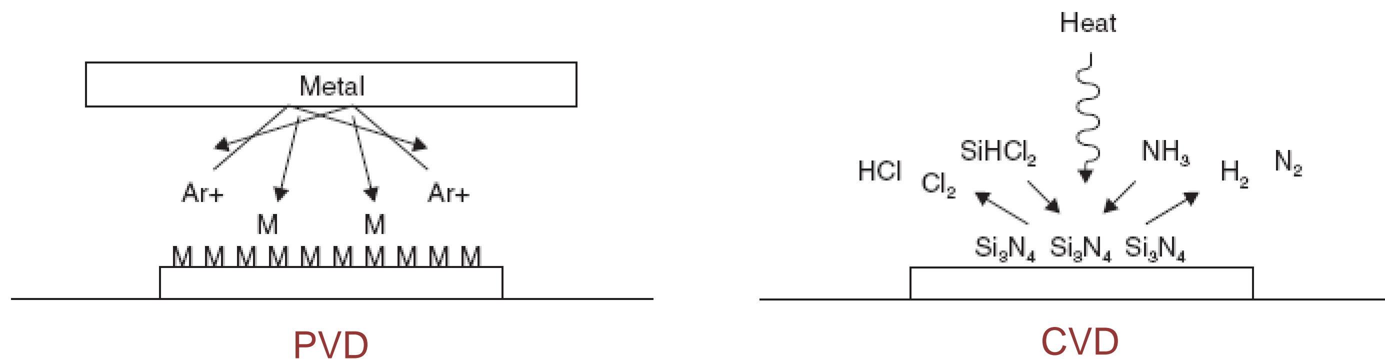
- In lift-off, the film to be patterned is deposited after the patterning is done – it is an additive process.
- The dissolution of the photoresist layer removes the supported films leaving only the film in the open PR region.
- The dissolution of the PR requires the solvent to have access to the PR layer, which is often helped by using an ultrasonic bath and by re-entrant PR sidewall profile.

- But you can also use your photoresist in direct association with a subtractive process.

Additive processes

Thin film deposition

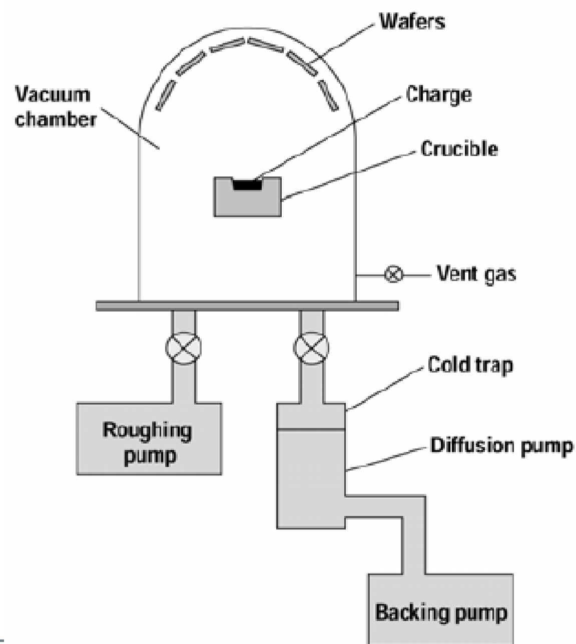
- Thin-film deposition is an additive process where a thin layer (nm-µm) of material is deposited over a substrate. Depending on the technique used we identify:
  - Physical Deposition: where simple deposition occurs by mechanical means.
  - Chemical Deposition: where a chemical reaction takes place on the substrate surface.



- There are many physical vapor deposition (PVD) techniques, where a vapor of the material to be deposited is condensing on the substrate, that are usually differentiated by the method used to vaporize the material :
  - Evaporation: using thermal energy.
  - Sputtering: using high energy ions from a plasma.
  - Cathodic arc deposition: use arc (a kind of very high energy plasma) created by electrical field, requires filtering to remove cluster of atoms
  - Pulsed laser deposition: using laser beam, etc…

Evaporation

- The simplest technique : high temperature heating vaporizes the material that condensates on the substrate
- Takes place at low pressure (between 10^{-5} and 10^{-7} Torr)
  - + High directionality, particularly well-suited for lift-off processes;
  - + Possible to obtain higher deposition rates than with other PVD methods.
  - – Poor adhesion.
  - – Does not work well for materials that do not vaporize as proper compounds:



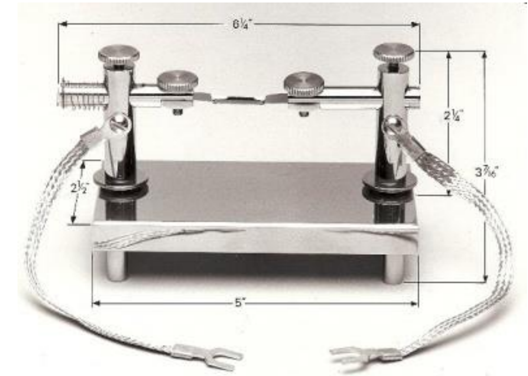
SiO_2 (solid) → SiO (vapor) +1/2 O_2

Al pellets

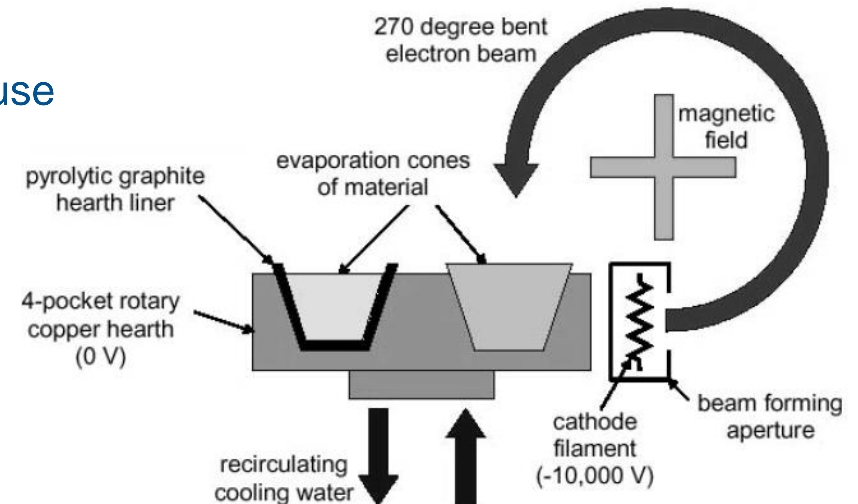
Silica

Evaporation

- Heating can be achieved by different techniques
  - Joule's heating in tungsten boat, through the material if it is conductive or inside heated crucibles.
    - Fairly inexpensive, but difficult to control.

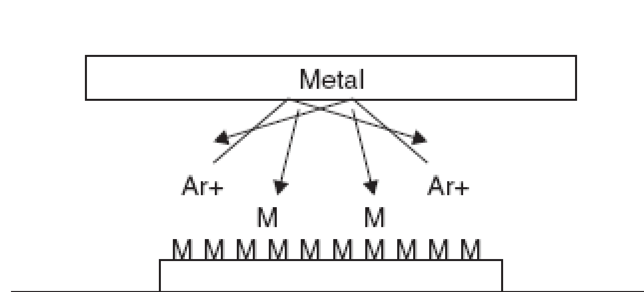


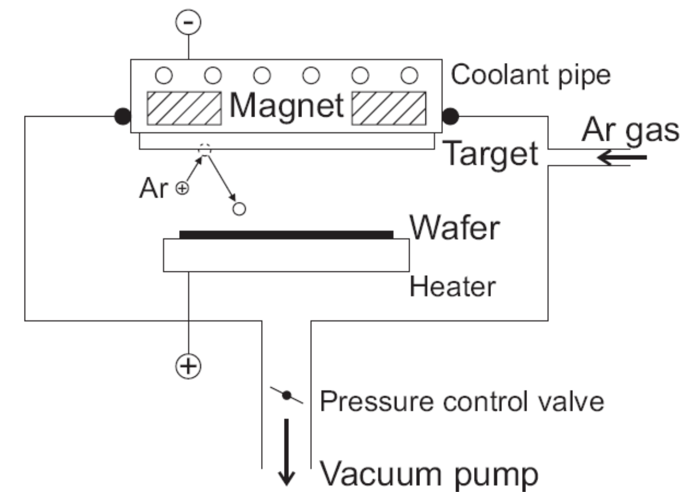
  - Electron beam heating: an intense e-beam is generated through a filament and steered via magnetic fields to strike the source material.
    - Highest temperature can be reached;
    - Finer control of the deposition process, but may cause high energy radiation exposure.



Sputtering

- The most common PVD process.
- A plasma is used to generate high energy ions which mechanically removes neutral atoms from the surface of a target with the desired material.
- The neutral atoms then fly through the plasma and condensate on the substrate.





- Sputtering has some advantages over evaporation:
  - All material can be sputtered;
  - Better adhesion;
  - More control over film stress.
- But evaporation cannot be beaten for lift-off processes and deposition rates (although rates can be improved using magnetron sputtering)!

Reactive Sputtering

- Sputtering in the presence of a gas (or a mixture of gases, Ar being generally maintained anyway).
- Higher rates than the one obtained when sputtering compounds directly (part. true for ceramics that require RF sputtering).
- Widely used technique for deposition of piezoelectric thin films (e.g. AlN and ZnO).
- Possible control of the composition (stoichiometry), but expect some issues…
  - Includes oxygen contamination through water (gas lines, chamber, etc…) in certain cases (does not matter for ZnO, obviously!)
- Control of the structure cannot only occur by controlling the process parameters: structure/texture of the substrate matters!
  - Importance of the "seed layer", particularly when looking for specific material properties
- The introduced gas reacts will all unpassivated surfaces, including chamber walls… and target:
  - Target poisoning: careful control of the deposition conditions required, limited time window for optimal operation.

Layer Modification

A few words on Si oxidation

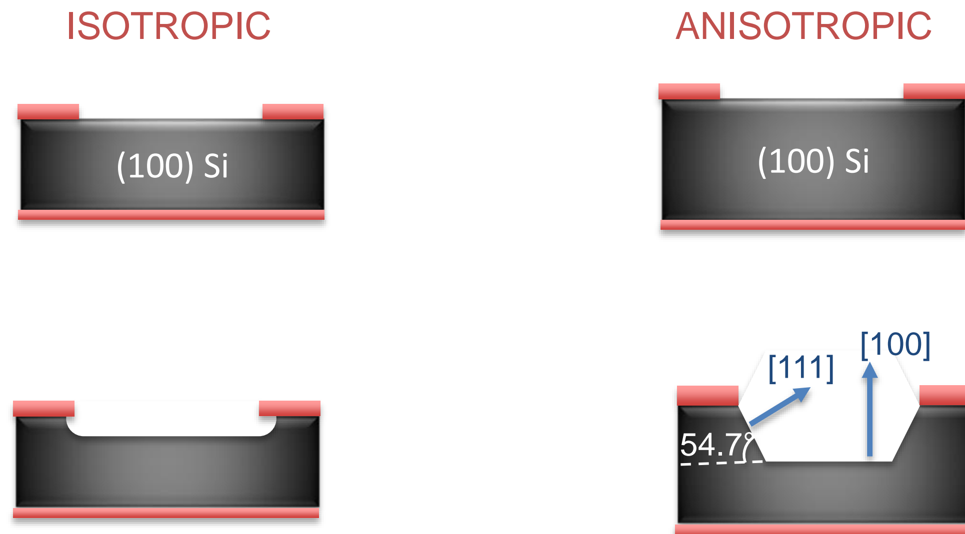
- Oxidation is a reactive growth process.
- The wafer is placed in a furnace at high temperature to grow silicon oxide in presence of oxygen in the form of a gas (O_2 – dry oxidation) or of water vapor (H_2O – wet oxidation).
- Oxidation happens at room temperature (“native oxide”), but high temperature facilitates the diffusion of oxygen.
- It is a layer modification process as the growth of a thickness of silicon oxide results in consumption of Si (just like iron rusting…) . Growth occurs while leaving a very clean Si/SiO_2 interface.
- Key process in microelectronics/MEMS, because of the very rich properties of SiO_2:
  - Stable down to 10^{-9} Torr , T > 900°C.
  - Can be etched with HF which leaves Si unaffected: great sacrificial layer!
  - Diffusion barrier for dopants.
  - Good insulator with a high dielectric breakdown field.

Subtractive processes

Etching

Subtractive process where material is removed from the layer to pattern

- Generally divided in two categories:
  - Wet etching: liquid solutions are used to remove the material through chemical reaction;
  - Dry etching: gas are used to remove the material chemically, physically or through the association of chemical and physical processes.
- In both cases, etching can be isotropic (all directions etched at the same rate) or anisotropic (for crystals only in the case of wet etching), meaning that etching occurs preferentially along specific directions.



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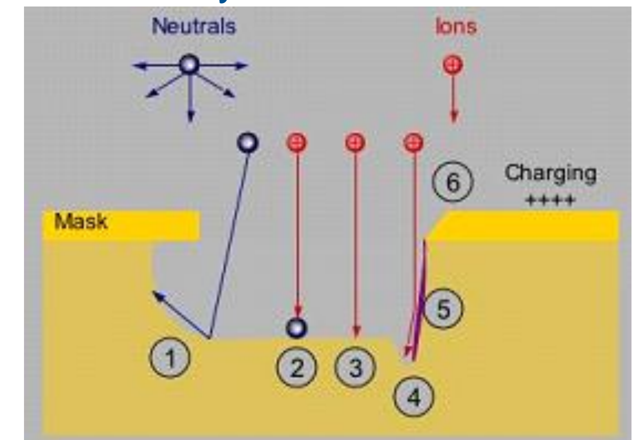
Wet etching

(Yes, the same as the one used for post-17th century engravings)

- In wet etching, the patterned wafers are immersed in the appropriate thermostated and agitated chemical bath placed on a wet bench under laminar flow and/or aspiration.
- The origin of the etching is purely chemical, with the etchant (or etching solution) reacting with the layer material.
- In general for the process to remove material, the chemical reaction with the solid phase layer should result in reacted species in the boundary layer that dissolves or turn into gas.
- Because of particle contamination issues and difficulty to reach dimension <1µm, wet etching is not used often anymore in microelectronics – but its low cost makes it very attractive in MEMS where dimension is not an issue.
- Some nice references regarding wet etching:
  - K. R. Williams & R. S. Muller, Etch rates for micromachining processing. *Journal of Microelectromechanical systems*, **5**, 256-269 (1996).
  - K. R. Williams, K. Gupta, & M. Wasilik, Etch rates for micromachining processing-Part II. *Journal of microelectromechanical systems*, **12**, 761-778, (2003).
  - http://www.cleanroom.byu.edu/wet_etch.phtml

Dry etching

- Dry etching is another subtractive process where gaseous species are used to etch the substrate
- For dry etching to work, the gas used should:
  - React with the material to be etched;
  - Result in volatile byproduct with low vapor pressure.
- To increase the etching rate, the process usually uses a plasma, that is, an electrically neutral and dense medium of high speed (temperature) electrons, with ionized and neutral atoms.
  - Ions can be accelerated by the electric fields at the bounding edges of the plasma so that they strike the surface.
  - Free radicals (uncharged) can diffuse to the surface and undergo reaction.
- Different mechanism explain the etching in a plasma and will occur simultaneously
  - Chemical etching by neutrals: isotropic, selective.
  - Ion enhanced etching by ions: anisotropic, selective.
  - Physical etching by ions: anisotropic, non-selective.



Dry etching

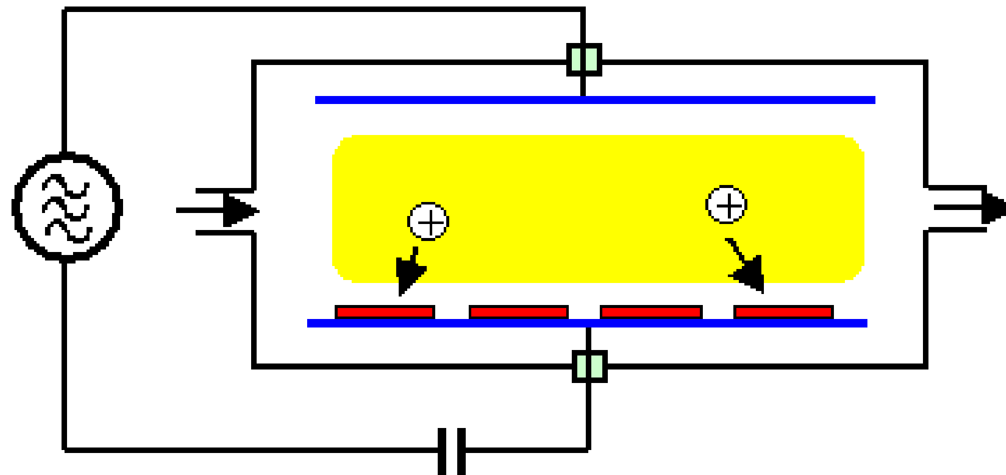
- Other phenomena affecting etching:
  - Trenching: ions deflected by sidewall overetch the bottom of the sidewall.
  - Passivation: deposition of by-product on sidewall, main cause of anisotropic etching.
  - Mask erosion: sputtering of mask by ions, resulting in reduced selectivity.

- Depending on the predominance of one of the etching mechanism, plasma based techniques can be divided in 3 categories
- Plasma etching: particles with low energy, work at higher pressure: mostly chemical removal.
- Reactive Ion Etching (RIE): particles with intermediate energy, large mean-free path to enhance etching anisotropy: physical and chemical removal.
- Ion milling: particles with high energy: essentially physical removal.

- Most materials can be plasma etched: the art is in achieving suitable selectivity both for masking layers and to layers that lie beneath the layer being etched.

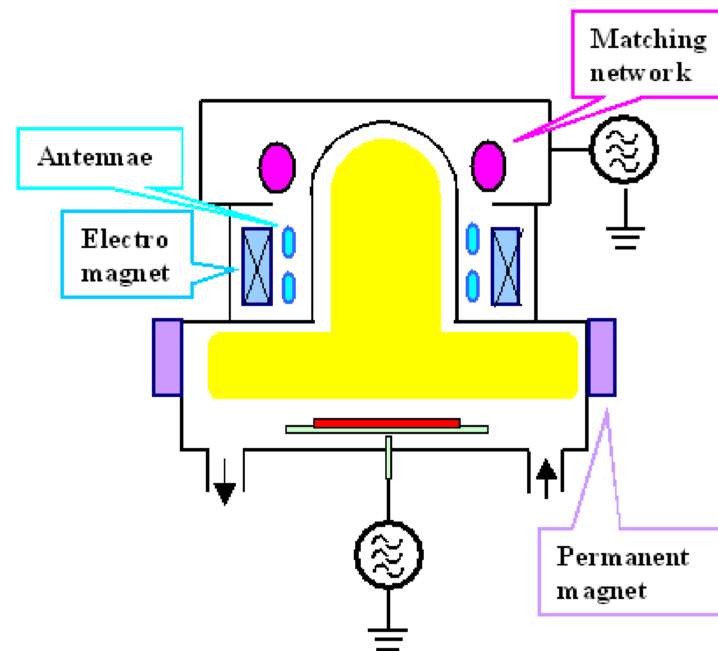
Reactive Ion Etching

- Both radicals (chemical reaction) and ions (bombardment) are generated in the plasma.
- Etching depends on reaction followed by creation of a gaseous byproduct which is pumped away.
- In the capacitively coupled (CCP) parallel plate configuration (i.e. "classical" RIE), gas is fed continuously in the chamber, the plasma is created by RF power and the field is due to bias (self or applied bias) of the lower electrodes because it is not grounded (coupled through a capacitor). The wafer is placed near the cathode to receive the energetic positive ions
- The presence of ion bombardment is able to increase tremendously the etching rate, even when ions are neutral atoms, supposedly by changing the surface roughness and energy.



Deep Reactive Ion Etching

- Uses inductively coupled plasma (ICP) combined with an additional electrode on the substrate holder:
  - Generation of reactive radicals.
  - Ion acceleration.
- Obtain simultaneously high plasma density and control ions energy without damaging the substrate.
- Greater control, much higher etching rate (~10µm/min compared to 1µm/min)



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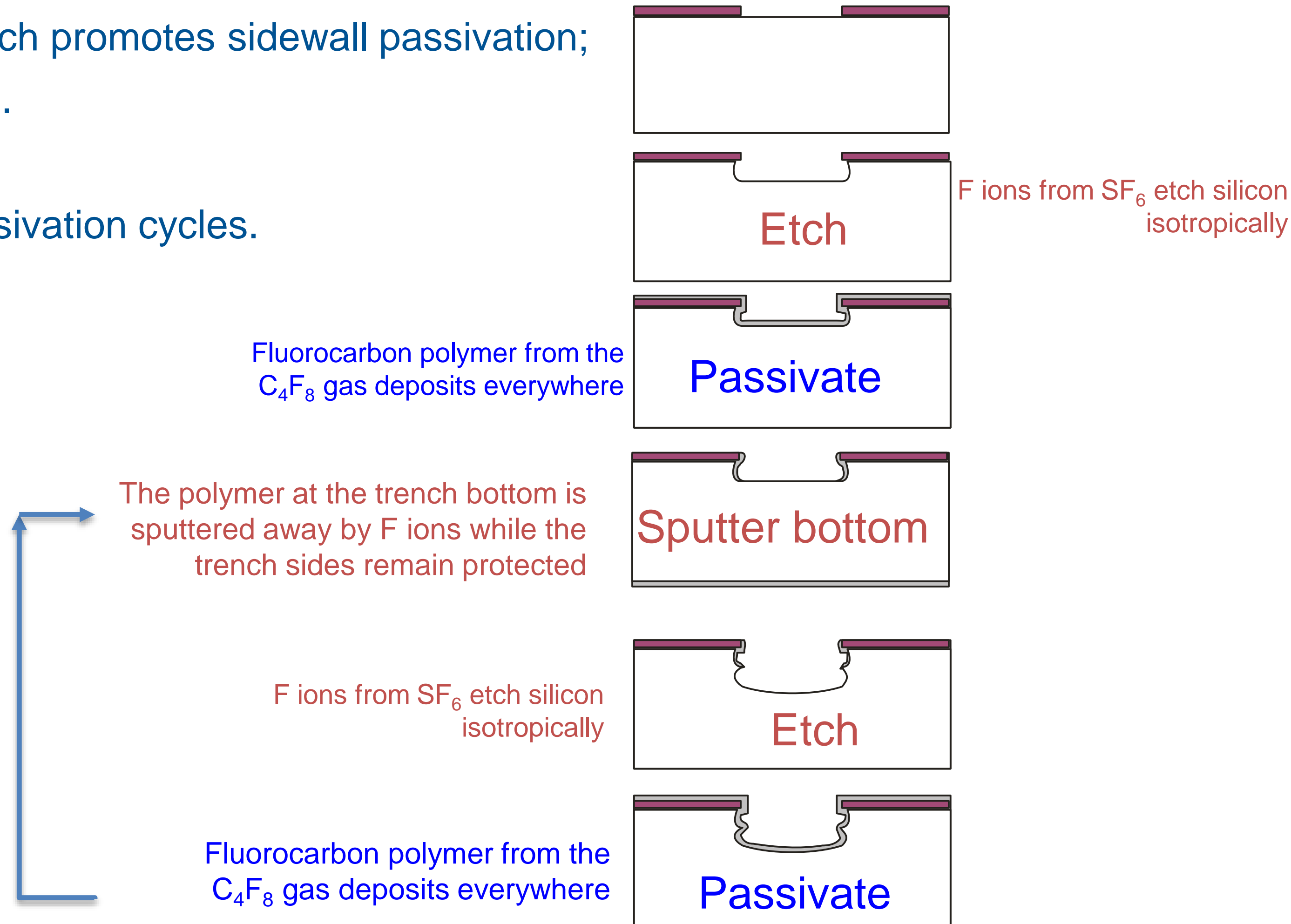
Deep Reactive Ion Etching

If the ICP process allows fast etching and thus potentially deep etch, it does not improve the anisotropy. Improving the anisotropy can be obtained by using:

- low temperature (-180˚C) which promotes sidewall passivation;
- the Bosch process (patented).

- Relies on alternating etch and passivation cycles.
- Gas used:
  - Etching : SF_6
  - Passivation : C_4F_8



Etching characteristics

Etch rate
The speed at which the material is etched (nm/min).

Selectivity
the ratio between the etching rate of the material and the mask (or another material).

Lateral etch ratio
An evaluation of the difference in etching rate between the horizontal and the vertical direction.

Aspect ratio
Used to characterize anisotropy. Defined as the ratio between the feature depth and width.

	Wet Etching	Dry Etching
Etching Method	Chemical with liquids	Physical and Chemical with gaseous species
Advantage	1) Low cost, easy to implement. 2) High etching rate and throughput. 3) Good selectivity for most materials. 4) Anisotropic with crystalline materials (along crystal axis direction).	1) Capable of defining small feature size (< 100 nm). 2) Anisotropic (vertical).
Drawback	1) Inadequate for small feature size <1µm. 2) Isotropic (in general). 3) Handling and environmental hazards. 4) Wafer contamination issues.	1) High cost, hard to implement. 2) Low throughput. 3) Poor selectivity. 4) Potential radiation damage.

Pattern Transfer Quick Test

A mask has the pattern shown in (a). Which photoresist and pattern transfer technique could be used to pattern the black thin film as shown in (b)?

1. positive photoresist and lift-off
2. negative photoresist and wet etching
3. positive photoresist and dry etching
4. negative photoresist and lift-off

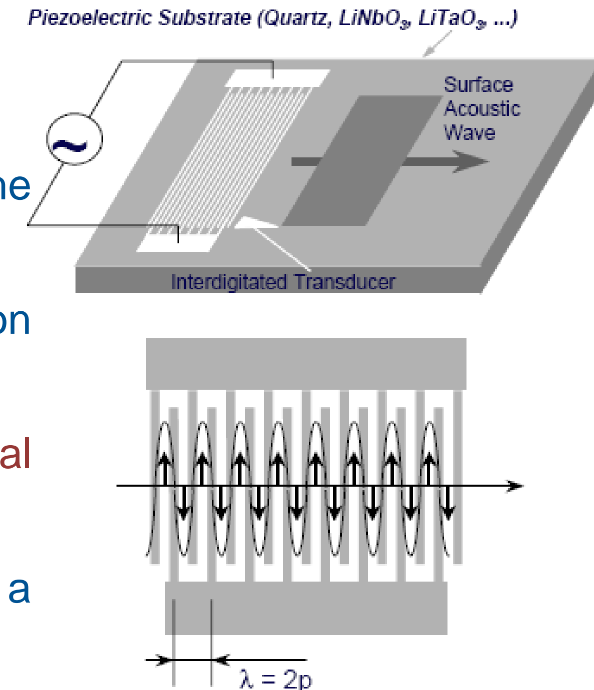
Application to RF devices

At last!

Substrates for Phononics (1)

Silicon is a fantastic material… but it is not piezoelectric

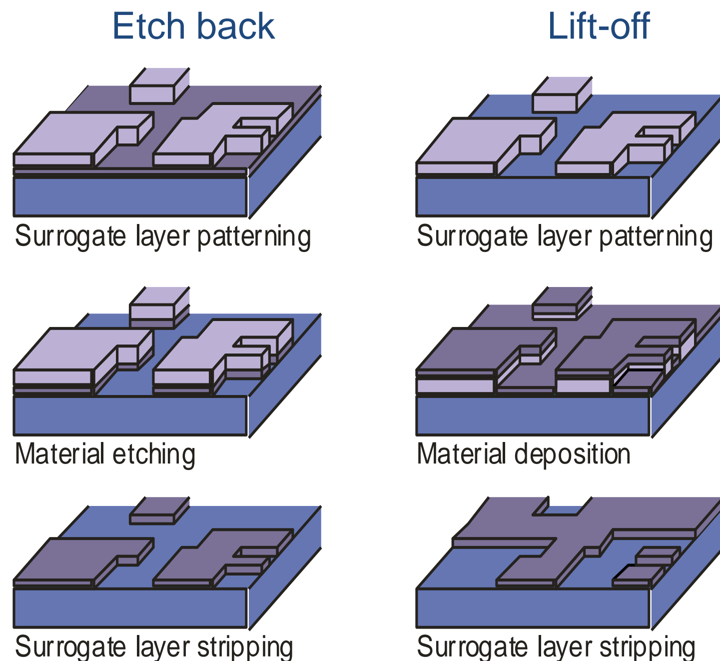
- SAW devices make use of single-crystal piezoelectric materials
  - SAW excitation through interdigital electrodes, *simply* lying atop the substrate surface.
  - Quartz, lithium niobate ($LiNbO_3$), lithium tantalate ($LiTaO_3$)… non CMOS-compatible!
  - High purity and hence high Q-factors (quartz), high electromechanical coefficients ($LixxO_3$)
  - Possibility to exploit the material anisotropy: interesting properties as a function of the crystal orientation:
    - Diffraction-less propagation, low temperature dependency, different wave propagation properties: SAWs, leaky SAWs…
    - Very fancy "crystal cuts": forget about using Miller indices to define substrate orientation and welcome the IEEE Standard on Piezoelectricity: $LiTaO_3$ Y+34/42, $LiNbO_3$ Y+128… Actually (YXwlt)/φ/θ/ψ.
    - Downside: micromachining…



Interdigital Transducers

Simple is beautiful

- Interdigital transducers rely on an extremely simple technology and are incredibly robust. Basically, they can be fabricated by a simple lift-off or etch-back process.



But, very high precision required !

3800 m/s at 2.45 GHz means l=390 nm !

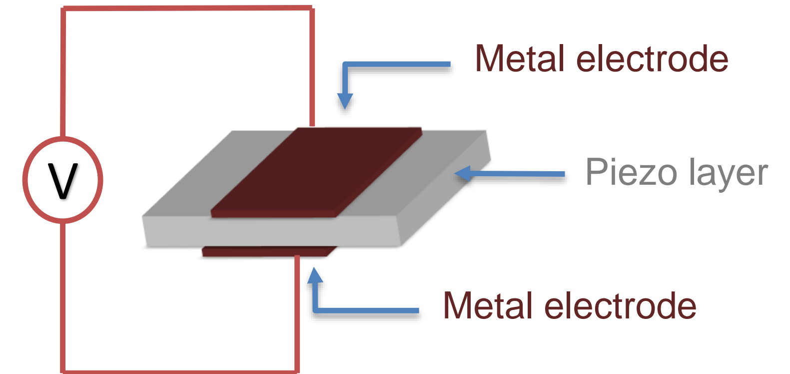
- Required resolution: about 0.38 µm à 2.4 GHz, with stepper limit that used to be 0.35 µm a few years ago (now moving to 0.2 µm).
- A SAW filter response is highly sensitive to:
  - Metal thickness: ± 1%.
  - Metallization ratio: needs to be controlled within a few %.
  - Electrode shape: underetch is not negligible.

➡ Grow thin film then grind to the appropriate thickness by in-situ monitoring.

➡ Use dry-etching.

Substrates for Phononics (2)

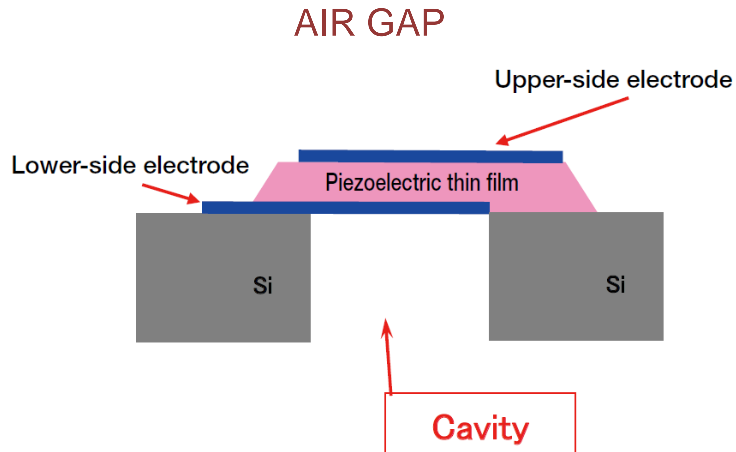
- RF bulk wave devices exploit waves propagating vertically: operation on a thickness mode of a piezo layer sandwiched between two metal electrodes.



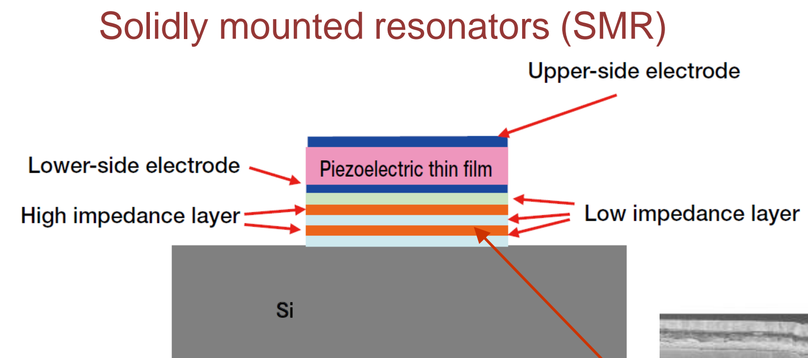
- High operating frequencies require thin piezo layer: forget about using a bulk substrate ($f = \frac{v}{2e}$).
  - Use piezoelectric thin films (< 1 µm) grown on a Si substrate and benefit from Si based technologies!!

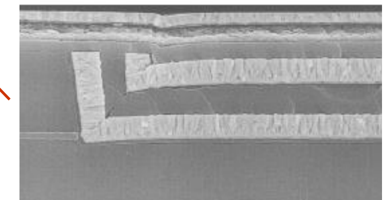
- Two families of film bulk acoustic wave resonators (FBARs)

AIR GAP



Solidly mounted resonators (SMR)





- Downside: low electro-mechanical coefficients, epitaxial growth limits orientation.

Easy FBAR

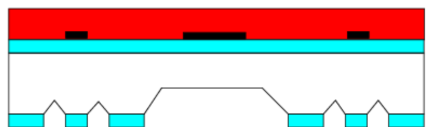
Let us increase the complexity a tad…

Thermal oxidation

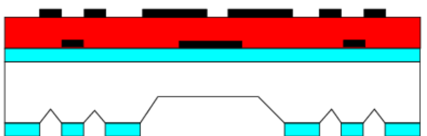
Open oxide

Si wet etching

Bottom electrode deposition

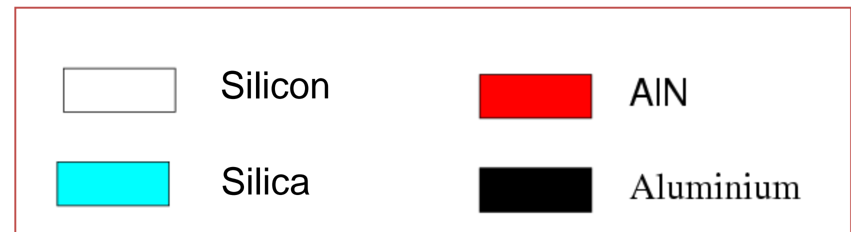


AlN deposition



Top electrode deposition

- Fairly simpl(istic)e air gap FBAR fabrication process.
  - 4 lithography steps;
  - 4 subtractive process steps;
  - 4 additive process steps;
  - 3 masks.



Almost real-life FBAR (Reality is worse…)

Courtesy of A. Reinhardt, CEA-LETI.

Cleaning, Bragg mirror dep, CMP, seed layer dep.

Ir dep. (counter electrode).

Litho, RIE of Ir through PR mask, PR striping.

AlN dep., Mo dep.

Litho, RIE of Mo through PR mask, PR striping.

Litho, wet etching of AlN through PR mask, PR stripping.

SiO_2 dep. (CVD…)

Litho, wet etching of SiO_2 through PR mask, PR stripping.

SiN dep. (CVD…)

Litho, RIE of SiN through PR mask, PR stripping.

AlCu dep.

Litho, wet etching of AlCu through PR mask, PR striping.

\+ Examples of (common) non planar topographies!

Substrates for Phononics (3)

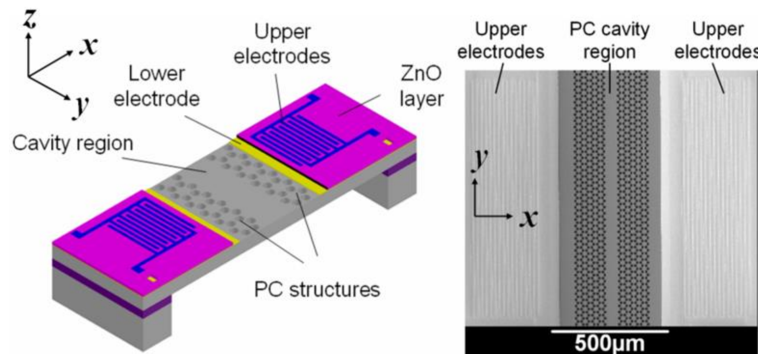
- Attempts to merge the best of two worlds: single-crystal wafer transport
  - Take a single-crystal bulk piezoelectric substrate, any crystal cut, any substrate;
  - Take a bulk Si substrate;
  - Bond them together;
  - Grind, lap, polish the single crystal wafer down to 1 µm.

Sounds easy, hmm?

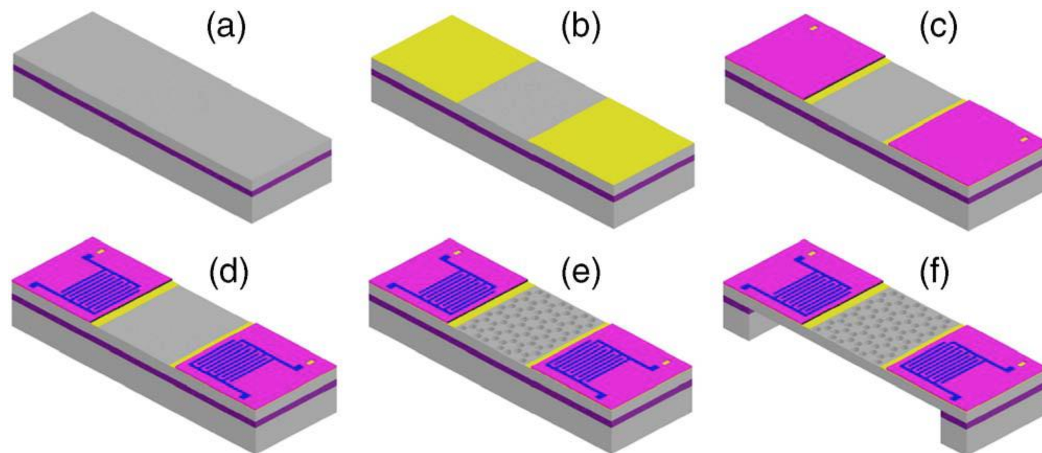
- Inspired from the *Smart-Cut* technology used to fabricate the so-called SOI wafers (silicon-on-insulator) but…
  - Bonding between distinct materials is an issue (and piezozlectricity+pyroelectricity does not help!)
  - The Smart-Cut techniques relies on ion implantation: heavy to implement.
  - Lapping and polishing down to a few 100's nm is easier said than done…

Si Phononic Crystal Slab

Let us put things the way colleagues at Georgia Tech did and discuss around that a bit.



a = 15 µm, r = 6.4 µm.
Membrane thickness: 15 µm.
Operating frequency: 120 MHz.



a) Start with an SOI wafer: a substrate of choice for Lamb wave devices!

b) |Au lower electrode/seed layer deposition and patterning (100 nm) using a lift-off process.

c) ZnO deposition through RF sputtering and patterning through an etch-back process.

d) Al top electrode deposition and patterning.

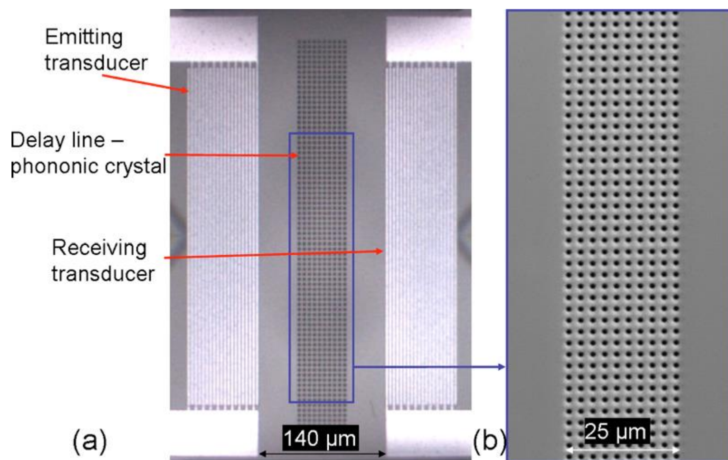
e) Holes: UV lithography + ICP etching.

f) Backside lithography and etching of Si substrate through ICP etching; etching of buried oxide layer.

S. Mohammadi; A. A. Eftekhar; W. D. Hunt; A. Adibi, *Appl. Phys. Lett.* **94**, 051906 (2009).

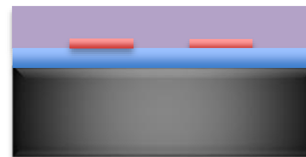
AlN Phononic Crystal Slab

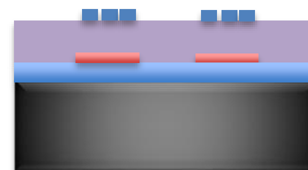
AlN acts as both the transduction layer and the propagating medium.

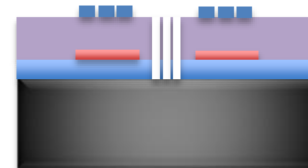


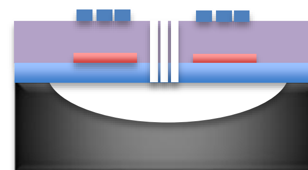
a = 6.6 µm, r = 2 µm.
Membrane thickness: 2 µm.
Operating frequency: 800 MHz.

M. Gorisse, A. Reinhardt *et al.* ,
Appl. Phys. Lett. **94**, 051906 (2009).









a) Start with Si wafer, perform SiO_2 oxidation.

b) Mo lower electrode/seed layer deposition and patterning using RIE.

c) AlN deposition through RF sputtering.

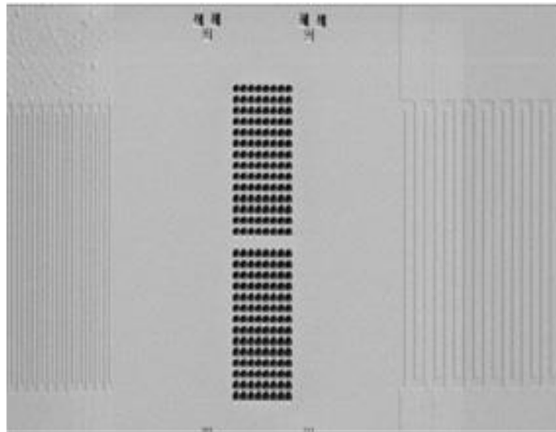
d) Al top electrode deposition and patterning using RIE.

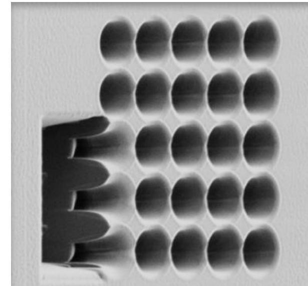
e) Holes: ICP etching through SiO_2 mask.

f) Membrane release through XeF_2 dry etching.

Monolithic SAW Phononic Crystal

Main issue: etching.

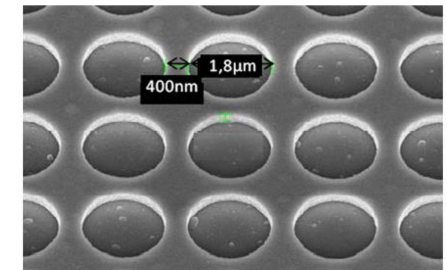


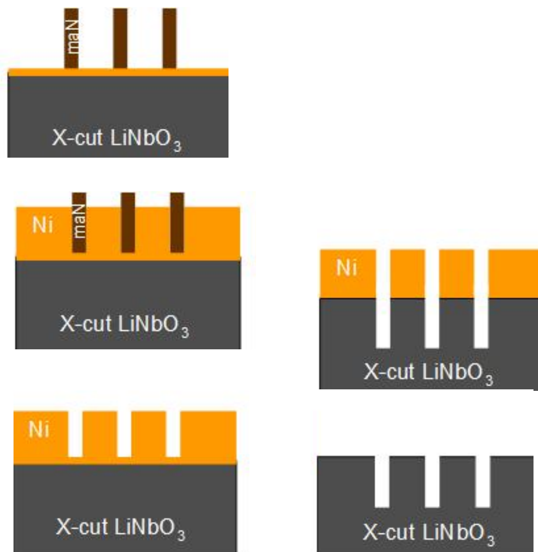


a = 2.2 µm, r = 1 µm.
Operating frequency: 800 MHz.

a) Al electrodes definition: e-beam lithography + lift-off.

b) Holes: direct focused ion beam milling.





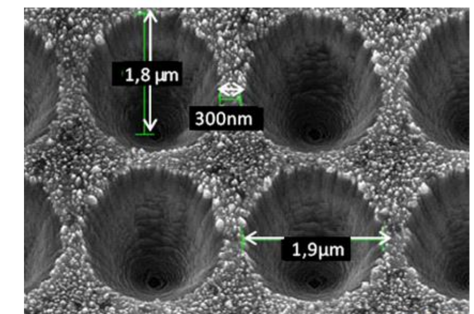
a) E-beam lithography for hole patter transfer.

b) Ni electroplating.

c) Reactive ion etching.

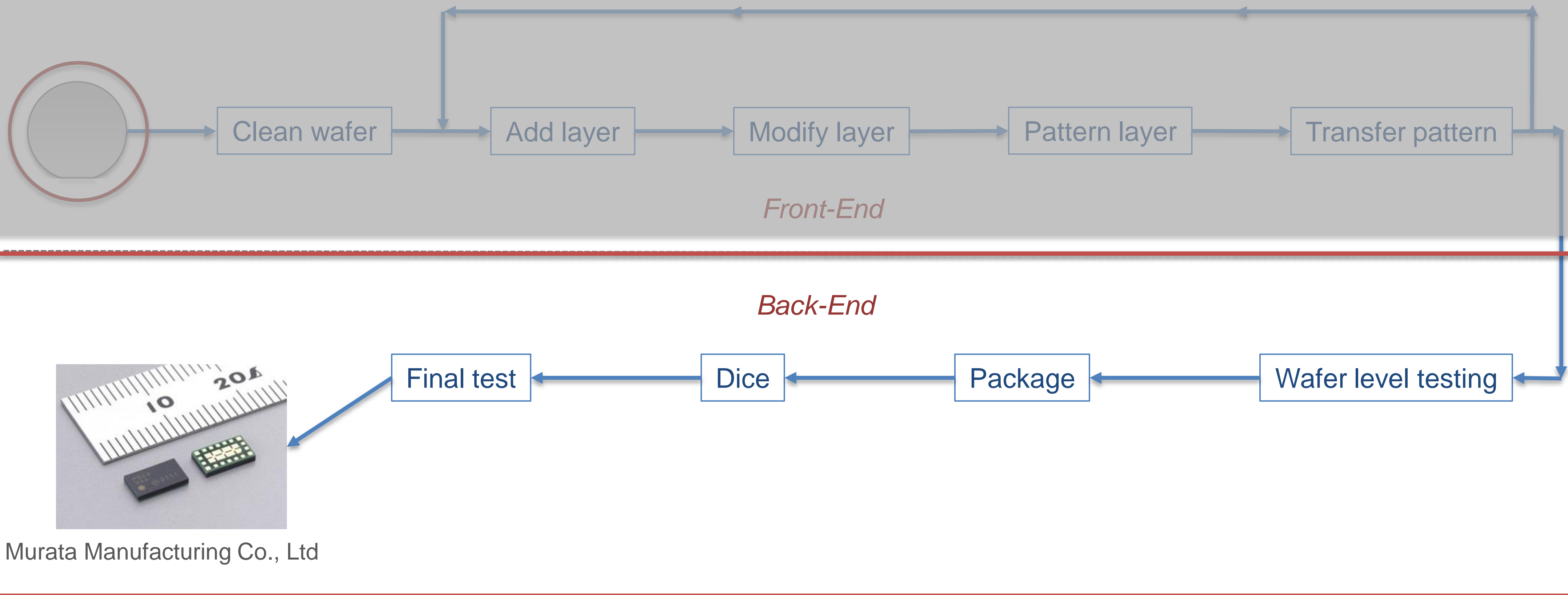
d) Ni mask stripping.

e) Al electrodes definition: e-beam lithography + lift-off.

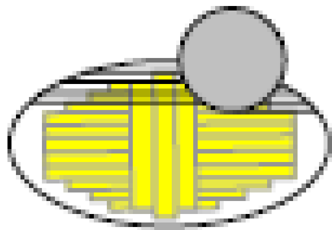


What about back-end?

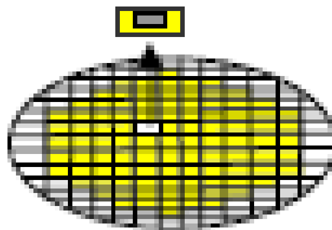
Remember our little wanna-be “generic” process flow?



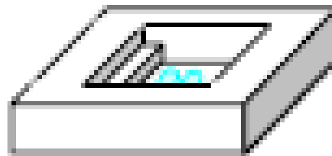
Surface Mount Component



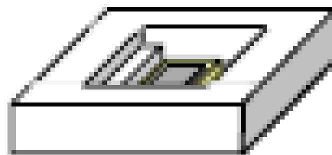
Wafer Dicing



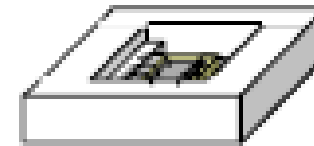
Chip collecting



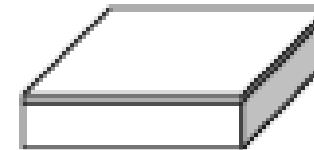
Adhesive coating



Die bonding



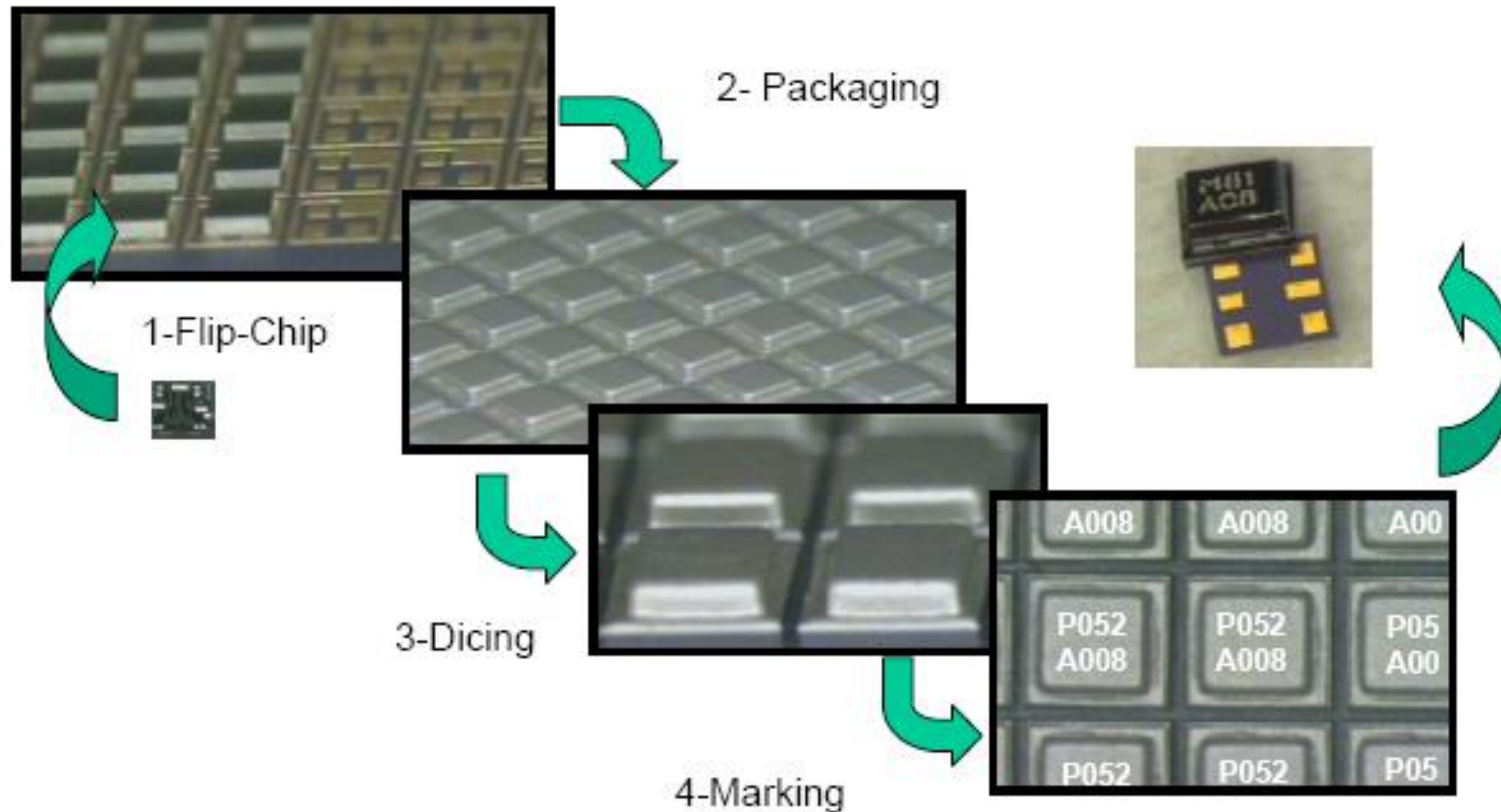
Wire bonding



Encapsulation

Marking

Wafer Level Packaging



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Conclusion

There are no specific technologies for RF Phononics

- Pick-up what you need from conventional MEMS processes.
  - “Simple” processes can be piled up to get very complex devices. Still…
    - There is a limit to how you can pile things up.
    - Every technological step has its own bounds.
      - Awareness of technological constraints is a pre-requisite (compatibility of process steps, achievable resolutions or aspect ratios, etc..)
      - Importance of the process flow: a clean room process cannot be improvised and built on the fly.
      - As a consequence, importance of the mask layout…
  - Lithography is the most important (but less visible) process step, it is at the heart of all.
- Phononic crystals are already at the resolution limit of stepper lithography: RF metamaterials are a very long way ahead indeed !